IN THE CLAIMS:

1. (Currently Amended) A control loop circuit for optimizing a power supply output under varying load conditions, the power supply having a main loop amplifier and an output stage to generate the output, the control loop circuit including:

a ~~static~~ first control path having a predetermined level of linear compensation, the first control path coupled to the output and having an error amplifier, the error amplifier operative to generate an error signal for presentation to the main loop amplifier, the error signal representing the difference between a desired output and a sensed output; and

a ~~dynamic~~ second control path coupled to the error amplifier output and responsive to the error signal to generate a dynamic compensation signal, the ~~dynamic~~ second control path having an output coupled to the main loop amplifier output.

2. (Currently Amended) A control loop circuit according to claim 1 wherein the ~~dynamic~~ second control path includes:

input conversion circuitry for converting the error signal into a digital signal,

a digital-signal-processor coupled to the conversion circuitry;

a look-up table for storing optimal compensation signal responses to detected error signals, the ~~DSP~~ digital-signal-processor operative in response to the digitized error signal to access the look-up table and identify the optimal compensation signal, and generating the optimal signal; and

output conversion circuitry for feeding the optimal signal to the main loop amplifier output.

3. (Original) A control loop circuit according to claim 2 wherein:

the look-up table comprises a RAM memory.

4. (Currently Amended) A control loop circuit according to claim 1 wherein the ~~dynamic~~ second control path is disposed in parallel with the ~~static~~ first control path.

5. (Currently Amended) A control loop circuit according to claim 1 wherein:

the ~~dynamic~~ second control path is selectively activated when the error signal is greater than a predetermined threshold.

6. (Original) A control loop circuit according to claim 2 wherein:

the output conversion circuitry comprises a digital-to-analog converter.

7. (Currently Amended) A control loop circuit according to claim 2 wherein:

the ~~static~~ first control path includes respective source and sink signal paths; and

the output conversion circuitry comprises respective source and sink digital-to-analog converters coupled to the respective source and sink signal paths.

8. (Currently Amended) A control loop circuit for controlling the loaded output of a DUT power supply, the DUT power supply including an input, a main loop amplifier and an output stage amplifier, the control system including:

means for statically ~~generating~~ compensating an error signal, ~~and~~ the means for statically compensating coupled between the input and output of the power supply; and

a dynamic compensation control loop including a digital-signal-processor, the dynamic compensation control loop disposed in parallel with the ~~static control loop~~means for statically compensating, the dynamic compensation control loop selectively cooperating with the ~~static control loop~~means for statically compensating to optimize the power supply output in response to varying output loads.

9. (Currently Amended) A control loop circuit according to claim 8 wherein:

the means for statically ~~generating~~ compensating an error signal comprises a ~~static~~ first control path having a predetermined level of linear compensation, the first control path including an error amplifier, the error amplifier operative to generate an error signal for presentation to the main loop amplifier.

10. (Currently Amended) A power supply system including:

a main loop amplifier circuit;

an output stage disposed in cascade with the main loop amplifier circuit; and

a control loop circuit, the control loop circuit including

a ~~static~~ first control path having a predetermined level of linear compensation, the first control path coupled to the output stage and having an error amplifier, the error amplifier operative to generate an error signal for presentation to the main loop amplifier, the error signal representing the difference between a desired output and a sensed output; and

a ~~dynamic~~ second control path coupled to the error amplifier output and responsive to the error signal to generate a dynamic compensation signal, the ~~dynamic~~ second control path having an output coupled to the main loop amplifier output.

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11. (Currently Amended) A ~~control loop circuit~~power supply system according to claim 10 wherein the ~~dynamic~~ second control path includes:

input conversion circuitry for converting the error signal into a digital signal,

a digital-signal-processor coupled to the conversion circuitry;

a look-up table for storing optimal compensation signal responses to detected error signals, the ~~DSP~~ digital-signal-processor operative in response to the digitized error signal to access the look-up table and identify the optimal compensation signal, and generating the optimal signal; and

output conversion circuitry for feeding the optimal signal to the main loop amplifier output.

12. (Currently Amended) A ~~control loop circuit~~power supply system according to claim 11 wherein:

the look-up table comprises a RAM memory.

13. (Currently Amended) A ~~control loop circuit~~power supply system according to claim 10 wherein the ~~dynamic~~ second control path is disposed in parallel with the ~~static~~ first control path.

14. (Currently Amended) A ~~control loop circuit~~power supply system according to claim 10 wherein:

the ~~dynamic~~ second control path is selectively activated when the error signal is greater than a predetermined threshold.

15. (Currently Amended) A ~~control loop circuit~~power supply system according to claim 11 wherein:

the output conversion circuitry comprises a digital-to-analog converter.

16. (Currently Amended) A ~~control loop circuit~~power supply system according to claim 11 wherein:

the ~~static~~ first control path includes respective source and sink signal paths; and

the output conversion circuitry comprises respective source and sink digital-to-analog converters coupled to the respective source and sink signal paths.

17. (Currently Amended) A method of controlling the output of a DUT power supply, the method including the steps of:

generating a statically compensated error signal based on the difference between the desired power supply output and the actual power supply output;

producing a dynamically compensated error signal in parallel with the statically compensated error signal; and

summing the statically compensated error signal and the dynamically compensated error signals to create an optimal compensation signal.

18. (Currently Amended) A method according to claim 17 wherein the producing step is dependent on the magnitude of the statically compensated error signal being above a pre-set threshold.

19. (Currently Amended) A method according to claim 17 wherein the producing step includes the steps of:

converting the statically compensated error signal into a digital signal;

analyzing the digital signal;

creating a digital dynamically compensated error signal based on the analyzing step; and

converting the digital dynamically compensated error signal to an analog dynamically compensated error signal.

IN THE SPECIFICATION: Please amend the specification as follows:

Page 3, lines 6 - 30:

To realize the foregoing advantages, the invention in one form comprises a control loop circuit for optimizing a power supply output under varying load conditions. The power supply has a main loop amplifier and an output stage to generate the output. The control loop circuit includes a ~~static~~ first control path having a predetermined level of linear compensation. The first control path is coupled to the output and ~~having~~ has an error amplifier. The error amplifier is operative to generate an error signal for presentation to the main loop amplifier where the error signal represents the difference between a desired output and a sensed output. A ~~dynamic~~ second control path is coupled to the error amplifier output and is responsive to the error signal to generate a dynamic compensation signal. The ~~dynamic~~ second control path has an output coupled to the main loop amplifier output.

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In another form, the invention comprises a power supply system including a main loop amplifier circuit and an output stage disposed in cascade with the main loop amplifier circuit. The system also includes a control loop circuit including a ~~static~~ first control path having a predetermined level of linear compensation. The first control path is coupled to the output stage and ~~having~~ has an error amplifier. The error amplifier is operative to generate an error signal for presentation to the main loop amplifier, the error signal representing the difference between a desired output and a sensed output. A ~~dynamic~~ second control path is coupled to the error amplifier output and is responsive to the error signal to generate a dynamic compensation signal, the ~~dynamic~~ second control path having an output coupled to the main loop amplifier output.

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In yet another form the invention comprises a method of controlling the output of a DUT power supply. The method includes the steps of generating a statically compensated error signal based on the difference between the desired power supply output and the actual power supply output;— producing a dynamically compensated error signal in parallel with the statically compensated error signal; and summing the statically compensated error signal and the dynamically compensated error signals to create an optimal compensation signal.

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Page 5, lines 2 - 15:

Control circuitry plays an important role in the ability of a high-accuracy power supply to maintain a desired voltage to a varying load under operating conditions. With reference to Figure 1, the control circuit of the present invention, generally designated 10, provides automatic optimal control compensation for powering a load 12 by combining a ~~static~~ first control loop 20 having a pre-set level of linear compensation with a compensation-programmable ~~dynamic~~ second control loop 70. This unique combination avoids fixed compensation settings and automatically adjusts the compensation to minimize manual input and errors.

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Generally, and further referring to Figure 1, the ~~static~~ first control loop 20 includes a main loop amplifier circuit 40 cascaded with an output stage circuit 50. An error amplifier circuit 30 feeds back the output from the output stage circuit to the input of the main loop amplifier circuit. The ~~dynamic~~ second control loop 70 also employs the error amplifier for its initial error signal and a digital-signal-processor (DSP) circuit 72 that is disposed in parallel with the main loop amplifier circuit.

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Page 6, lines 10-35, Page 7, lines 1-4:

The inventors have discovered that by adding the ~~dynamic~~ second control loop in parallel with the statically compensated first control loop, changes in compensation to the error signal to provide optimal performance may be automatically provided without external manual intervention. As noted briefly above, the ~~dynamic~~ second control loop 70 includes a DSP circuit 72. The DSP circuit includes a digital signal processor 74 and memory 76 (either on or off-chip) for storing look-up tables, algorithms, and the like. An analog-to-digital converter ADC1 is coupled to the output of the error amplifier 32 to sample the analog error signal and present it in digital form to the DSP circuit. An inverse setup is provided at the DSP output with a pair of digital-to-analog converters DAC1 and DAC2 to convert digital source or sink signals to analog waveforms for presentation through resistors R11 and R12 to the negative inputs of the drivers U3 and U4.

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In operation, the force signal converter DAC1 provides the desired supply voltage level to the error amplifier circuit 30. Changes in current demand by the DUT 14 are sensed along the sense lines 22 and 24 to the inputs of the error amplifier 32, and the

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actual level compared to the desired level. The difference is then fed to the rest of the ~~static~~ first control loop 20, and the ~~dynamic~~ second control loop 70 simultaneously.

The main loop amplifier circuit 40 acts on the error signal to provide the pre-set level of linear compensation defined by the values of Rcomp and Ccomp. The resulting signal is then fed through to the rectifier 52 and directed along either the source or sink signal path 64 or 66, depending on the signal polarity. This linear compensation signal from the first control loop is then augmented with a dynamic compensation signal from the ~~dynamic~~ second control loop 70 as more fully described below.

As the ~~static~~ first control loop 20 responds to the error signal, the DSP 74 receives a digitized version through the converter ADC1. The digital signal is then analyzed over a series of samples to determine the optimum level of compensation for the power supply. In effect, the DSP and its associated algorithm can effectively implement a much higher order filter function than the simple RC scheme in a normal control loop, and it does it with a constant phase delay unlike a higher order filter implemented in analog components.

Page 7, lines 10-15:

Preferably, when the error amplifier signal goes below a threshold value, the output of the ~~dynamic~~ second control loop 70 should be zero. The main analog amplifier circuit 40 is under control of the loop. The DSP 74 only becomes active to provide dynamic response optimization during periods of time where the error amplifier 32 detects errors above a threshold value. This allows the statically compensated first control loop 20 to provide optimal accuracy during periods of static or slowly changing conditions.